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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/581,849	10/16/2007	Gunther Leising	U 016328-0	4589

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EXAMINER
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ART UNIT	PAPER NUMBER
2883	

NOTIFICATION DATE	DELIVERY MODE
02/11/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/581,849	LEISING ET AL.	
	Examiner	Art Unit	
	ROBERT TAVLYKAEV	2883	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-23,26-28,30,32,34,42-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-23,26-28,30,32,34,42-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/30/10*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/15/10 has been entered. Claim 21 has been amended. Claims 21 – 23, 26 – 28, 30, 32, 34, and 42 – 49 are pending.

Information Disclosure Statement

2. The information disclosure statement filed 9/30/10 at least in part fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to all of the cited foreign patent documents but one has not been considered.

Applicant Request for Interview

3. The Examiner called Attorney Raymond DiPerna (Reg. No. 44,063) on 2/4/11 and informed him that a new ground(s) of rejection would be applied. The parties agreed that an interview, if needed, would be scheduled after Applicant's review of the new ground(s) of rejection.

Response to Arguments

4. Applicant's arguments regarding the rejections under 35 USC 103(a) have been fully considered but they are moot in view of the new grounds of rejections, as necessitated by Applicant's amendments. In particular, the added limitation "measuring distances on the printed circuit board element as presently formed" has necessitated an updated search which yielded a reference by Elchelberger et al (EP 0273703 A2), the latter being combined with Bennion et al (GB 2155194 A) to comprehensively disclose all of the limitations recited by amended claim 21.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in Graham **v.** John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bennion et al (GB 2155194 A) in view of Elchelberger et al (EP 0273703 A2).

Regarding claim 21, Bennion discloses (e.g., Figs. 1 – 3 and 5; Abstract; page 1, lines 35 – 41) a direct-write laser system and a corresponding method for producing an optical circuit board element, the method comprising the steps of:

mounting at least one optoelectronic component (e.g., a laser (10) and a modulator (12)) to a substrate (14);

subsequently applying to the substrate an optical layer (20), comprised of an optical material changing its refractive index under photon irradiation, while at least partially embedding the optoelectronic component in the optical layer;

subsequently controlling a radiation unit (comprising a UV laser (51) and a computer-controlled translation stage) including a lens system (54) to displace a focal area of an emitted laser beam in a plane the optical circuit board element, and adjusting the focal area also in terms of a depth within the optical layer (page 2, lines 55 – 60); and

thereafter producing an optical waveguide structure (comprising (22)) adjoining the optoelectronic component (Fig. 3) within the optical layer by photon irradiation, the optical

waveguide structure (22) being surrounded by the remaining optical layer (20).

Bennion cites (e.g., page 2, lines 60 – 61) that there can be a unit for determining an absolute position of the optical circuit board element but does not cite that the latter can be a printed circuit board element and does not detail a variety of possible alternative implementations of such a position determining unit, even though a variety of direct-write laser systems with visual feedback and position determination are well-known in the art and would have been an obvious choice to a person of ordinary skill in the art. In this regard, Elchelberger discloses (e.g., Fig. 1; page 5, lines 7 – 26; page 9, lines 38 – 47; page 10, lines 4 – 47) a system that comprises an optical vision and targeting unit (comprising a camera (26), computer (32), (control electronics (34), and an x-y table (30)) and that is used to establish interconnections between components of a printed circuit board element (page 2, lines 36 – 39), which comprises a plurality of components mounted on a common substrate. It would have been obvious to a person of ordinary skill in the art that the method for producing a circuit board element disclosed by Bennion can include an additional step of using an optical vision and targeting unit to determine a position of the optoelectronic component (laser (10) and/or modulator (12) in Fig. 1 of Bennion) embedded in the optical layer (20) and measure distances (e.g., between a plurality of components; page 9, lines 38 – 47 of Elchelberger) on the printed circuit board element as presently formed, as disclosed by Elchelberger. The motivation is that deviations of the actual position(s) of the at least one optoelectronic component from a designed value(s) can be measured and used to correct/adjust the positions of the optical waveguide structure adjoining the at least one optoelectronic component thereby reducing/eliminating a possible undesirable offset between the optical waveguide structure and the at least one optoelectronic component and

hence reducing the corresponding optical coupling loss.

Regarding claim 22, Bennion discloses (e.g., a laser (10) and a modulator (12) in Fig. 1) that there can be at least two optoelectronic components mounted to the substrate, embedded in the optical layer, thereafter are connected with each another by the optical waveguide directly adjoining the same (Fig. 3).

8. Claims 23, 26, 27, 32, 42 – 46, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bennion et al (GB 2155194 A) in view of Elchelberger et al (EP 0273703 A2), as applied to claim 21, and further in view of Iwaki et al (US Pub. No. 2004/0001661 A1).

Regarding claim 23, the Bennion – Elchelberger combination does not provide details of the printed circuit board (PCB) element, even though PCBs and their construction are well-known in the art. In this regard, Iwaki discloses (e.g., Figs. 1 and 15) a printed circuit board (PCB) element including at least one optical waveguide (105) provided in an optical layer (106/104) and at least one optoelectronic component (103) that is in optical connection with the optical waveguide (105) and embedded in the optical layer (106). Iwaki states (par. [0048] and [0054]) that the optical waveguide (105) can be formed/structured by photon (UV) irradiation within the optical layer (106), the latter being formed of a photorefractive material. Iwaki cites (par. [0054]) that the refractive index of the photorefractive material changes (increases) under photon irradiation, thereby producing an optical waveguide structure (comprising an optical waveguide core that provides light confinement) surrounded by the remaining optical layer and adjoining the optoelectronic component (103). As an aside, it is noted that the teachings of Iwaki

render obvious a method of producing the PCB element that at least partially overlaps with the steps recited by claim 21, as was detailed in the Office Action of 4/14/10. Further, Fig. 7B of Iwaki shows that after the production of the optical waveguide structure (105) in the optical layer (106), a printed circuit board layer (119) including a conductive inner ply (comprising the parts (121a) and (121c)) is applied to at least one side of the optical layer (106). It would have been obvious to a person of ordinary skill in the art that the PCB element disclosed by the Bennion – Elchelberger combination can have the construction (including a conductive inner ply) illustrated by Iwaki. The motivation is that printed circuit boards having complex optical and electrical interconnections and performing optoelectronic processing can be enabled and used in a variety of systems, including high-speed optical communication systems (e.g., par. [0004] of Iwaki).

Regarding claim 26, Fig. 6 of Iwaki shows that vias (comprising (140) and (125)) are provided in the optical layer (104) and in the printed circuit board layer (129a), in coordination with the respective optoelectronic component (103), and that electrically conductive connections to the optoelectronic component can be established through the vias.

Regarding claim 27, Fig. 8 of Iwaki shows that the optoelectronic component (103) is conductively connected with an associated electronic component, i.e. a driving part (113). Fig. 8 does not explicitly show a printed circuit layer or a substrate. However, it would have been obvious to a person of ordinary skill in the art that there can be a printed circuit layer (which is included between the part (113) and the optical layer (106) and is used for mounting the part (113)), because Iwaki illustrates such a printed circuit layer in Fig. 6 and teaches that this arrangement is desirable as providing increased mechanical stability/rigidity of the entire printed circuit board element (par. [0059] of Iwaki).

Regarding claims 42 and 43, Figs. 6 and 7B of Iwaki show that the inner ply (comprising the parts (121a) and (121c)) may be patterned before applying the printed circuit board layer ((119) or (129a)) to the optical layer (104). Figs. 6 and 7H - 7I show that the outer ply (comprising (121b) or (141)) can be patterned after such application.

Regarding claim 44, Iwaki teaches (par. [0085]) that the disclosed printed circuit board element can include multilayer boards on one of both sides of the optical layer. Two or more layers in a multilayer board can represent a cover layer and a substrate with the cover layer being provided before applying the optoelectronic component thereto.

Regarding claims 32, 45, and 46, Fig. 6 of Iwaki shows that electrical connections for the optoelectronic components (103) and (101) are established throughout an electrically conductive distribution layer (comprising parts (121a) and (121c)), the distribution layer being configured as a heat-dissipation layer. Fig. 6 makes it obvious that the distribution layer can be applied to a substrate (129a) and subsequently patterned.

Regarding claim 48, Fig. 15 of Iwaki discloses an optical waveguide (105) provided with a lens structure (109) on its end adjacent an optoelectronic component (101), the latter being a light reception device. The lens structure at least partially encloses the optoelectronic component (101) and is used for focusing light into the optoelectronic component (101). The focusing property depends on the refractive index of the material used to form the lens structure (109). Iwaki does not explicitly state that the lens structure (109) can be made a part of the optical waveguide (105). However, Iwaki does cite (see paragraph [0098]) that the refractive index of the material should be higher than that of the optical layer (104). Thus, it would have been obvious to a person of ordinary skill in the art that the material of the optical waveguide

(105) can be used to form the lens structure (109) and be integral with it, since the refractive index of optical waveguide (105) satisfies the above condition. The motivation for forming the lens structure (109) as a part of the optical waveguide (105) is that such a structure would have a reduced the number of needed materials, can be produced in a single step, and reduces cost, while still providing the benefit of an improved light collection efficiency.

9. Claims 28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bennion et al (GB 2155194 A) in view of Elchelberger et al (EP 0273703 A2) and further in view of Iwaki et al (US Pub. No. 2004/0001661 A1), as applied to claims 21 and 44 above, and further in view of Yoshimura et al (US Patent No. 6,684,007 B2).

Regarding claim 28, Fig. 8 of Iwaki shows that the optoelectronic component (103) is used with an associated electronic component, i.e. a driving component (113). In Fig. 8, the driving component (113) is shown to be positioned on one side of the board. However, Iwaki's invention also includes an embodiment, wherein the driving device (113) is arranged inside the board (par. [0085]), thus making it an embedded unit. The optoelectronic component (103) (e.g., a light emission device (see paragraph [0046])), if combined with the driving component (113) (i.e. an electronic driver), is an optoelectronic chip. Therefore, the Bennion – Elchelberger – Iwaki combination (see the arguments and motivation for modification as applied to claim 21 above) teaches all of the subject matter, except for stating that the optoelectronic component (103) may be combined to form a unit with an associate electronic component (113) (shown in Figs. 6 and 8). However, Yoshimura discloses a printed circuit board element, which may have a polymer optical waveguide, electrical layers, and vias, and teaches (see col. 62, lines 28-66) that

a VCSEL (optoelectronic device) with an integrated driver (electronic component) or a photodetector (optoelectronic device) with an integrated amplifier (electronic component) may also be used. Therefore, it would also have been obvious to a person of ordinary skill in the art that the optoelectronic component (103), which is embedded in the optical layer (104) and mounted to a substrate, as disclosed by Iwaki, can be combined to form an optoelectronic chip unit with an associate electronic component, as disclosed by Yoshimura. The motivation is that a smaller footprint and higher component packing density can be realized by such integration, compared to using individual components.

Regarding claim 30, Iwaki further teaches (par. [0065]) that some layers can be made of a light blocking material. Such material would absorb light. It would have been obvious to a person of ordinary skill in the art that if a substrate layer is made of a light blocking material, then a cover layer comprising an optically transparent material and acting as an optical buffer would be required to be applied to the substrate, in order to separate the light-absorbing substrate and the optical layer and avoid high optical loss. The motivation for such a substrate / cover layer combination is that both low-loss optical transmission and reduced optical cross-talk due to suppressed stray light (par. [0065] of Iwaki) can be obtained.

10. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bennion et al (GB 2155194 A) in view of Elchelberger et al (EP 0273703 A2) and further in view of Iwaki et al (US Pub. No. 2004/0001661 A1), as applied to claim 21 above, and further in view of Pollak et al (US Pat. # 5,255,070).

Regarding claim 34, the Bennion – Elchelberger – Iwaki combination teaches all the subject matter, except for explicitly stating that the optoelectronic component (103) can be produced in situ on the substrate by a thin-film technique. It is noted that a great variety of thin-film techniques, such as molecular beam epitaxy (MBE) and chemical vapor deposition (CVD), are well known in the art and would have been obvious to a person of ordinary skill in the art. In this regard, Pollak cites (col. 1, lines 14 – 24) that thin-film techniques (MBE and MOCVD) are routinely used for making optoelectronic components (e.g., quantum wells that are the key component of quantum-well lasers). Therefore, it would have been obvious to a person of ordinary skill in the art that the optoelectronic component (e.g., the laser (10) in Fig. 1 of Bennion) disclosed by the Bennion – Elchelberger – Iwaki combination can be produced in situ on the substrate by a thin-film technique. The motivation for using a thin-film technique is that it allows a simultaneous production of a number of optoelectronic components and can achieve high integration density.

11. Claims 47 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bennion et al (GB 2155194 A) in view of Elchelberger et al (EP 0273703 A2) and further in view of Iwaki et al (US Pub. No. 2004/0001661 A1), as applied to claim 21 above, and further in view of "Two-photon polymerization initiators for three-dimensional optical data storage and microfabrication," by Cumpston et al, Nature, vol. 398, March 1999, pp. 51 – 54 (hereinafter Cumpston).

Regarding claims 47 and 49, Fig. 15 of Iwaki discloses an optical waveguide (105) having a certain shape, e.g., with a lens structure (109) on its end adjacent an optoelectronic

component (101). Overall, the teachings of Bennion, Elchelberger, and Iwaki combine (see the arguments and motivation for modification as applied to claim 21 above) to teach all of the subject matter, except for detailing other possible shapes and structures of the optical waveguide formed by photon irradiation, even though a great variety of waveguide shapes are well known in the art and routinely used for various reasons. In this regard, Fig. 3c of Cumpston describes the formation of 3D optical waveguide structures with a higher refractive index and shows a tapered optical waveguide that is widened in a funnel-shaped manner. It is noted that tapered waveguides are well known in the art and used for coupling to optoelectronic components, such as semiconductor lasers. Cumpston further states (page 53, 3rd full paragraph) that the produced waveguide structures can be photonic bandgap structures, which are also known as photonic crystal structures. The latter are well known in the art as being capable of providing light confinement and mode shaping via a variety of topologies (lenses, tapers, etc.). Therefore, it would have been obvious to a person of ordinary skill in the art that the optical waveguide disclosed by the Bennion – Elchelberger – Iwaki combination can have various shapes and structures, including those recited by the claims and illustrated by Cumpston. Tapers are known to improve optical coupling between optical elements with different mode sizes, while photonic crystals additionally provide tight light confinement and enable sharp transitions, thereby minimizing a device footprint.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

"Nanostructuring in submicron-level waveguides with femtosecond laser pulses," by Li et al, Optics Communications, vol. 212, pp. 159 – 163, Oct 2002, describes a direct-write laser system with visual feedback and improved accuracy.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT TAVLYKAEV whose telephone number is (571)270-5634. The examiner can normally be reached on Mon - Thur 9 am - 6 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Robinson can be reached on (571)272-2319. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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2/5/11